The Phase Locked Loop.

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1. Introduction

The Phase-Locked Loop (PLL) is one of the most commonly used integrated circuits (ICs) in use in modern communications systems. Although perhaps surprisingly first invented as early as 1932 by Bellescise it never gain popularity until the early 1970s when cheap ICs were readily available. It quickly found application as a precision FM demodulator as a replacement for Foster-Seely discriminators. Digital communication systems quickly followed and the PLL has found application in such areas as modems, mobile communications, satellite receivers and television electronics. The PLL is used extensively in modern electronic systems but its design is often met with trepidation. This is perhaps understandable since to fully understand the operation of a PLL requires some knowledge of communication systems and control systems, two subjects which are treated in isolation. For example seldom are PLLs covered in a taught control course at undergraduate level whilst feedback and stability is only briefly mentioned when covering PLLs in a communication course. The two subjects need to come together and be treated seamlessly.
2. Basic PLL Theory

The block diagram of a generic PLL is shown in Figure 1 below.

Without loss of generality we consider an input to the PLL which is FM. Whilst there are other types of input which can be used this approach gives the option of modulating various different base-band signals which can be later used to test the PLL. For example a step input or a sinusoidal frequency response are commonly used for testing all feedback control systems. The FM signal which must be simulated has the analogue form $f(t)$ where

$$f(t) = \cos(\omega_c(t) + \Delta \omega \int \cos(\omega_m t) dt)$$  \hspace{1cm} (1)

where $\omega_c$ and $\omega_m$ are respectively the carrier and base-band frequencies in rad/s and $\Delta \omega$ is the depth of modulation measured in rad/s. When equation (1) is integrated it has the more familiar form

$$f(t) = \cos(\omega_c(t) + \beta \sin(\omega_m t))$$  \hspace{1cm} (2)

where $\beta = \Delta \omega / \omega_m$ is defined to be the FM modulation index. It should be noted that although equation (1) has an integration that this is implicit in its generation and no explicit integration is required in the simulation for FM generation. The approach used in [3] did require an integrator to simulate FM but this was because the simulation was an exact mathematical representation of (1). In LabVIEW it is possible to simulate directly an oscillator with a voltage controlled input (ie a voltage controlled oscillator or VCO). Hence the VCO block simulation is identical to real FM generation as will subsequently be shown.
The important thing to show with the VCO is that it has a transfer function which is a pure integrator[5]. A good analogy is to consider a block diagram of a motor whose output is position rather than velocity. An integrator $1/s$ block must be included in the block diagram and this in turn affects the stability of the closed-loop system. Similarly for a PLL the VCO has an input that is frequency and an output which is phase (that in turn feeds into the phase detector). Since phase is the integral of frequency it has a transfer function of the form

$$\frac{\phi}{\omega}(s) = \frac{K_s}{s}$$

(3)

where $\phi$, $\omega$, $K_s$ are respectively phase, frequency and the VCO gain. In an IC PLL an equation is often given for the VCO gain which will change if the free-running frequency is altered in any way (usually by an external C-R time constant). The free-running frequency in Figure 1 is matched to the carrier frequency of the incoming FM. If there is a small miss-match the demodulated FM will have an extra dc offset superimposed. If the miss-match is too big then lock cannot be achieved and hence it should be as close as possible to the carrier frequency of the FM signal.

The phase detector in an analogue PLL is normally a linear multiplier. In digital PLLs it can be an Exclusive–OR or some other similar method. Here we consider the case where the phase detector is a linear multiplier. When the PLL is in-lock the VCO output has to be in phase-quadrature with the incoming FM signal. For simplicity, consider the case when there is no FM and the input is sinusoidal. For this case the VCO output will have the same frequency but will have a 90 degrees phase shift relative to the incoming signal. One method of checking if a PLL is in-lock is to check for this phase-quadrature condition. Considering an instantaneous small phase shift to the incoming FM signal $\phi_{in}$ and similarly to the VCO output $\phi_o$, the phase detector output will become $e(t)$ where

$$e(t) = \cos(\omega_c t + \phi_{in} - 90) \cos(\omega_c t + \phi_o)$$

(4)

which when using basic trigometric angle reduction becomes

$$e(t) = 0.5[\sin(\phi_{in} - \phi_o) + \cos(2\omega_c t + \phi_{in} + \phi_o - 90)]$$

(5)

Examining (5) it can be seen that the term with $\cos()$ is at a frequency of twice the carrier frequency and if the bandwidth of the PLL is designed properly this term can be attenuated significantly. The other term in $\sin()$ for small angle changes is approximately a subtraction or phase error detection as required. The 0.5 scaling factor can be compensated for later with a suitable overall gain adjustment. The design of the filter is considered finally.
3. The Linear PLL Design

The beauty of the PLL is that it can be analysed in a linear form independent of the carrier frequency. The block diagram of the closed loop PLL is shown in Figure 2. The VCO transfer function $H(s)$ is shown as a pure integrator and the phase detector as a summing junction providing negative feedback. It remains to find the filter dynamics $F(s)$.

![Figure 2. Linear PLL](image)

To find the filter dynamics the open-loop Bode plot should have a similar form to the one shown in Figure 3.
This type of PLL is sometimes known as a third order type II PLL as there are two integrators within the loop. The first integrator is the VCO and the second is an added electronic integrator. Since two integrators with negative feedback results in an oscillator a phase lead (advance) stabilisation is needed. Hence the overall Bode plot has the form shown in figure two. This particular design is preferred as it has better tracking abilities than a type I PLL. The higher the gain at low frequencies results in good tracking and hence low error. The open-loop transfer function which describes Figure 3 is

\[ F(s)H(s) = \frac{K}{s^2} \frac{(1 + sT_1)}{(1 + sT_2)} \]  

(6)

the gain of the VCO has been absorbed into an overall gain term K. It should be pointed out that is also possible to design a PLL in other ways. For example if the time constant \( T_2 = 0 \) in (6) above the final –40dB/decade roll-off will no longer exist. However with that approach the filtering ability of the loop is not as good and hence the noise immunity suffers. Whilst it is possible to do more filtering outside the loop, the problem of too much \( 2\omega_c \) can cause problems with dc-offsets, distortion and the ability to lock. It is therefore desirable to get rid of as much carrier \( 2\omega_c \) feed-through.
as possible within the loop and do a mild amount of filtering outwith the loop. Setting $T_2 = 0$ does have an advantage however of giving a larger phase margin and hence better stability properties. A further discussion is given in Appendix 1.

The unity gain bandwidth of the PLL should be chosen high enough to track adequately but not too high so as to let too much $2\omega_c$ through. By experience it has been found that a unity gain bandwidth of

$$f_\phi = \frac{2f_c}{10}$$  \hspace{1cm} (7)

gives the best results.

Referring to Figure 3 the ratio

$$r = \frac{f_2}{f_1}$$  \hspace{1cm} (8)

is sometimes known as the ‘span ratio’, and determines the phase margin of the system and hence the stability of the loop [6]. For a phase lead network the phase margin for various $r$ values is found from

$$\phi_m = \sin^{-1} \left( \frac{r - 1}{r + 1} \right)$$  \hspace{1cm} (9)

Which for a span of $r=10$ gives a phase margin of approximately 55 degrees. A phase margin of 55 degrees is normally considered to give a good transient response. The frequency where the gain is unity is given by [6]

$$f_\phi = \sqrt{f_2 f_1}$$  \hspace{1cm} (10)

which is the geometric root of the upper and lower break-frequencies.

It is of importance to state that the bandwidth is normally fixed at the value given by (7) whilst the span ratio can be varied for different designs. For example a larger span ratio results in better stability at the expense of poorer tracking and vice versa. The rise-time or speed of response of the PLL is unaffected since it is assumed the bandwidth remains constant. The two time constants in (6) are found directly from the Bode plot to be

$$T_1 = \frac{1}{2\pi f_1}$$  \hspace{1cm} (11a)

$$T_2 = \frac{1}{2\pi f_2}$$  \hspace{1cm} (11b)

The upper and lower break-frequencies are found by using (10) and (8)

$$f_2 = f_\phi \sqrt{r}$$  \hspace{1cm} (12a)

$$f_1 = \frac{f_\phi}{\sqrt{r}}$$  \hspace{1cm} (12b)
To find the overall gain $K$ in (6) for a given span ration and time constants it is necessary to evaluate

$$\frac{K \ (1 + sT_1)}{s^2 (1 + sT_2)} = 1$$

(13)

evaluated at a frequency $\omega = \omega_\phi$ which is the unity gain frequency or bandwidth. After some algebra it can be shown that $K$ is found from

$$K = \frac{\omega_\phi^2}{r}$$

(14)

Example

The following example will be used in the simulation to follow. Suppose the carrier frequency is 2kHz. From (7) the unity gain bandwidth is 400Hz. Selecting a span ratio of $r=10$ for a good phase margin the upper and lower break frequencies of the Bode plot can then be evaluated as $f_1 = 1264$Hz and $f_1 = 126.4$Hz. From (11a and b) the time constants are evaluated as $T_1 = 1.259$ms and $T_2 = 0.1259$ms. The overall gain which must include any ‘hidden’ gain terms (the VCO and the 0.5 from the phase detector for instance) is found from (14) to be $K = \frac{\omega_\phi^2}{\sqrt{r}} = 1.9989 \times 10^4$. This gain is then split between the various parts of the PLL. The parts which already have built in (hidden) gain terms must be accounted for within this overall gain.

Monolithic PLL on a chip.

A real PLL (NE 565) which works on analogue FM is shown in Figure 4 below.
As shown in the figure, the PLL system consists of a phase detector or comparator (PC), a voltage-controlled oscillator (VCO), an amplifier and R-C combination forming low-pass filter circuit. The input signals are fed to the phase detector through pins 2 and 3 in differential mode. The input signals can be direct-coupled provided that the dc level at these two pins is made same and dc resistances seen from pins 2 and 3 are equal. By shorting pins 4 and 5 output of VCO is supplied back to the phase comparator (PC). The output of PC is internally connected to amplifier, the output of which is available at pins 6 and 7 through a resistor of 3.6 kΩ connected internally. A capacitor C₂ connected between pins 7 and 10 forms a low-pass filter with 3.6 kΩ resistor. The filter capacitor C₂ should be large enough so as to eliminate the variations in demodulated output and stabilize the VCO frequency. Voltage available at pin 7 is connected internally to VCO as a control signal. At pin 6 a reference voltage nominally equal to voltage at pin 7 is available allowing both the differential stages to be biased. Pins 1 and 10 are supply pins.

The centre frequency of the PLL is determined by the free-running frequency of the VCO which is given as

\[ F_{\text{out}} = \frac{1.2}{4R_1C_1} \text{ Hertz} \]

where R₁ and C₁ are external resistor and capacitor connected to pins 8 and 9 respectively, as illustrated in figure. The free-running frequency \( f_{\text{out}} \) of the VCO is adjusted, externally with R₁ and C₁, to be at the centre of the input frequency range. Resistor R₁ must have a value between 2 and 20 kilo ohm. Capacitor C₁ may have any value.

The 565 PLL can lock to and track an input signal typically ± 60 % bandwidth with respect to \( f_{\text{out}} \) as the centre frequency. The lock-range of PLL is given as

\[ f_L = \pm \frac{8f_{\text{out}}}{V} \text{ Hertz} \]
where $f_{out}$ is free-running frequency of VCO in Hz and $V = (+ V) – (- V)$ and capture range is given as

$$f_c = \pm \left[ \frac{f_L}{2\pi} \right] (3.6) (10)^3 C_2^{1/2}$$

The lock range usually increases with an increase in input voltage but falls with an increase in supply voltages.

If a linear element like a four-quadrant multiplier is used as the phase detector, and the loop filter and VCO are also analog elements, this is called an analogue, or linear PLL (LPLL).

If a digital phase detector (EXOR gate or J-K flip flop) is used, and everything else stays the same, the system is called a digital PLL (DPLL).

![Figure 5 Frequency scaling (upwards) using a PLL](image)

Referring to Figure 5, a system for using a PLL to generate higher frequencies than the input, the VCO oscillates at an angular frequency of $\omega_D$. A portion of this frequency/phase signal is fed back to the error detector, via a frequency divider with a ratio $1/N$. This divided-down frequency is fed to one input of the error detector. The other input in this example is a fixed reference frequency/phase. The error detector compares the signals at both inputs. When the two signal inputs are equal in phase and frequency, the error will be zero and the loop is said to be in a "locked" condition.

When $GH$ is much greater than 1, we can say that the closed loop transfer function for the PLL system is $N$ and so

$$F_{OUT} = N \times F_{REF}$$
Appendix 1 Variations of PLL design

This Appendix examines briefly three other types of PLL design which are often discussed in the literature. Consider first the Bode plot shown in Figure A1.

The transfer function of the filter for this kind of PLL has the form

\[ F(s) = \frac{K}{(1 + sT_f)} \]  \hspace{1cm} (A1)

which is just a first order low-pass filter. The problem with this approach is that the slope of the frequency response is only –20dB/decade and clearly at a given frequency below the unity gain bandwidth (assuming that the bandwidth is the same for all the examples herein) is less than for the case with an added integrator. The only integration is that of the VCO itself. The phase-margin and hence stability can be better than for the two integrator case with less overshoot. The tracking ability of this kind of loop is inferior to designs with a –40dB/decade slope at low frequencies.
Another approach is to add a second integrator as in the main text but to exclude the second −40dB/decade roll-off as shown in Figure A2.

It has good tracking abilities similar to the example in the main text and better phase-margin and hence stability. However, the exclusion of the second pole makes it more susceptible to noise and in particular the twice carrier frequency which is generated by the phase detector. Such a filter is often termed a proportional plus integral (P-I) controller.

Finally consider the most popular approach as used in many IC PLLs. A few external components can easily construct a lag-Lead filter of the form
the Bode plot is shown in Figure A3. The term lag-lead is a slight misuse of terminology as in fact (A3) is only a lag compensator (since $T_3 < T_2 < T_1$) with a high frequency pole. The complete Bode plot with the VCO integrator looks as if a lead compensator is present from $f_2$ and hence the name.

\[ F(s) = \frac{(1 + sT_3)K}{(1 + sT_1)(1 + sT_3)} \]  

(A3)

Figure A4 A type I third order PLL.

This design has good tracking properties at low frequencies at least as low as the frequency $f_1$ in Figure A4 and the rest of the frequency response above this frequency is identical to Figure 3 except that the phase margin is slightly better than the design with a pure integrator. For many IC PLLs the frequency $f_1$ is so low that the design is similar to having a pure integrator. Theoretically however with two integrators (the added integrator + the VCO inherent in the loop) the PLL should be
able to track ramping phase variations whereas with one only the VCO acting as the integrator there will always be a constant error.